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CAMPOS, YAIMA	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,718	THOMPSON ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/713,718 has a total of 20 claims pending in the application; there are 3 independent claims and 17 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

III. OBJECTIONS TO THE SPECIFICATION

CLAIM OBJECTIONS

4. **Claims 1, 2, 4, 6, 8, 12, 17 and 20** are objected to because of the following informalities:

5. As per **claim 1**, the word "at" in line 2 is believed to be a typographical error and has been treated as – **a** – for the rest of this office action.

It appears that the words "the data strobe" in claim 1, lines 5 and 11 should be corrected – **a data strobe**— and have been treated as such for the rest of this office action.

6. As per **claim 2**, it is believed that the words "the distribution rate" in lines 1-2 should be **–a distribution rate-** and have been treated as such for the rest of this office action.

It appears that the words "the rate" in line 2 should be **–a rate-** and have been treated as such for the rest of this office action.

7. As per **claim 4**, it is believed the punctuation of ";" at the end of the claim contains a typographical error and should be corrected to -- . --.

8. As per **claim 6**, it is believed that the words "the position" in line 3 should be **–a position-** and have been treated as such for the rest of this office action.

9. As per **claim 8**, because claim 1 refers to only one "memory cell," it is believed that the words "the memory cells" in line 1 should be **–a memory cell-** and have been treated as such for the rest of this office action.

It appears that the words "the data pulse" in line 10 should be **–a data pulse-** and have been treated as such for the rest of this office action.

10. As per **claim 12**, it is believed that the words "the data signal" in line 5 should be **–a data signal-** and have been treated as such for the rest of this office action.

11. As per **claim 17**, it is believed that the words "the fraction portion" in lines 3-4 should be **–a fractional portion-** and have been treated as such for the rest of this office action.

It appears that the words "the read data pulse" in line 13 should be **–a read data pulse-** and have been treated as such for the rest of this office action.

12. As per **claim 20**, it is believed that the words "fraction portion" in lines 1-2 should be **–fractional portion-** and have been treated as such for the rest of this office action.

13. Appropriate correction is required.

IV. REJECTIONS NOT BASED ON PRIOR ART

a. DEFICIENCIES IN THE CLAIMED SUBJECT MATTER

Claim Rejections - 35 USC § 101

14. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

15. **Claims 2-3** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

16. As per **claim 2**, this claim is directed to both, "the system of claim 1" (line 1) and a "process for measuring distribution rate" (lines 1-2); therefore, Claim 2 is directed to neither a "process" nor a "machine," but rather embraces or overlaps two different statutory classes of invention set forth in 35 U.S.C. 101 which is drafted so as to set forth the statutory classes of invention in the alternative only.

17. Any claim not specifically addressed above is being rejected as encompassing the deficiencies of a claim upon which it depends.

Claim Rejections - 35 USC § 112

18. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

19. **Claims 2-3 and 11-16** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

20. As per **claim 2**, this claim is directed to both, "the system of claim 1" (line 1) and a "process for measuring distribution rate" (lines 1-2) which renders this claim ambiguous and indefinite under 112, second paragraph. Applicant might consider amending claim 2 to be directed to "the system of claim 1" and contain references to the process in which "the system of claim 1" is intended to be used, as long as it is clear that the claim is directed to the system and not the process.

21. **Claim 11** recites the limitation "the rank of the DDR memory component" in line 2. There is insufficient antecedent basis for this limitation in the claim. The applicants might consider amending this claim to read – **a rank of a DDR memory component** --.

22. **Claim 13** recites the limitation "the command tenure" in line 1. There is insufficient antecedent basis for this limitation in the claim. The applicants might consider amending this claim to read – **a command tenure** --.

23. Any claim not specifically addressed above is being rejected as encompassing the deficiencies of a claim upon which it depends.

V. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. **Claims 1-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gustavson et al. (US 6,442,644) in view of Olarig (US 6,134,638).

26. As per **claim 1**, Gustavson discloses "A system, comprising: a table comprising at first timing adjustment signal associated with a rank of a memory component" as a **["fine-and-coarse tunable delay element of fig. 1b, namely 112b (BkRd) represents at least the latency delay of IAMU (*individually addressable memory unit*) 111 for a given bank read operation where the bank read operation generally requires the selecting or opening of a specific bank" wherein "the delay of tunable BkRd delay element 112b may be increased by the command module 150' to provide a longer delay as appropriate for scheduling bank-read bursts" (Column 20, lines 40-48). Gustavson discloses having a table to define time adjustments as "device-internal registers and other memory may be used for storing local ID codes, calibration values and other information" wherein device characteristics information comprises "number of banks" and "delay values" (Table 2.5 and Column 37, lines 55-63) and explains that "in response to command module 150' placing a code representing the current frequency of CCLK in the 'Frequency register' of a given SLDRAM module, the latter module will generally alter the characteristic information (e.g., min/max delay times) it provide on the read-only side of its LCM (*local configuration memory*)" (Column 38, lines 56-61)]** "and a second timing adjustment signal associated with the memory component;" **[With respect to this limitation, Gustavson discloses "a page read latency value is associated with IAMU (*individually addressable memory unit*) 111. In fig. 1b such a PgRd latency is associated with coarse-and-tunable delay element 112a. This tunable PgRd delay 112a indicates at minimum how much time it would take to read and already-opened row (a**

page) within an already opened bank after a page-read command packet is issued by command module 150'. The delay of tunable PgRd delay element 112a may be increased by the command module 150' to provide a longer delay as appropriate for scheduling page-read bursts" (Column 20, lines 24-39)] "a pipeline for imparting a gross timing delay for adjusting the data strobe signal associated with the memory component using a first portion of the first timing adjustment signal; and a memory cell connected to the pipeline operable for: receiving at least a second portion of the first timing adjustment signal," **[Gustavson discloses this concept as "In the actual device, the tunable delay is usually established by vernier shifting of phases of internal clocks that strobe respective latches of the data pipeline instead of using analog delay elements. However, any kind of delay technology may be used as appropriate" (Column 20, lines 50-56) and explains that "a memory device may be divided into separate bank groups, each servicing a different DataLink and concurrent operation may be obtained with pipelined commands" (Column 50, lines 20-23) wherein "the in-circuit memory controller" is allowed to make "command adjustments (e.g. individual phase changes) to the delay elements such as 112a, b" (Column 21, lines 26-27); specifying "SLDRAM module 120' has its own set of separately tunable delay/phase means and its own set of SLIO receivers (*Synchronous Link Input/Output*) (for data read) and (for command receive)" (Column 22, lines 27-30)]**.

Gustavson does not disclose expressly "adjusting the data strobe signal using the second portion by an amount less than the amount of the first portion."

Olarig discloses "adjusting the data strobe signal using the second portion by an amount less than the amount of the first portion" as **[a system in which "the memory clock signals may**

include different frequencies and thus allow different speed SDRAM's to be used" having "memory clock generator" programmed "to provide an appropriate clock frequency based on" data that "identifies the type of SDRAM included in each bank" (Columns 4-5, lines 66-67 and 1-5). Olarig also teaches that "clock generator 500 preferably is provided with the system clock from which the clock generator derives SDRAM clock frequencies. A number of frequency multipliers and frequency dividers are used in conjunction with multiplexers 506, 530 for selecting an appropriate clock frequency" (Figure 6 and Column 11, lines 43-46) as being able to adjust timing signals by different amounts; for example, being able to produce a greater amount when multiplying or smaller amoubt when dividing by any integer].

Gustavson et al. (US 6,442,644) and Olarig (US 6,134,638) are analogous art because they are from the same field of endeavor of controlling timing signals used for computer memory access and control.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the computer memory system which applies timing adjustments to memory banks as well as to components within each memory bank as taught by Gustavson and further adjust timing signals by different amounts as taught by Olarig.

The motivation for doing so would have been because Olarig teaches that adjusting memory control timing signals by different amounts **[provides the advantage of reducing computer system cost as consumers are able to "re-use" older "memory devices in new computer systems" when "upgrading to a new computer system" (Column 2, lines 39-42); providing a system that is "capable of implementing memory devices with different**

operating speed," therefore, optimizing the "performance of each memory device by performing transaction at the fastest possible speed with each memory circuit" (Column 2, lines 60-67 as "the memory clock signals may include different frequencies and thus allow different speed SDRAM's to be used in computer system" (Columns 4-5, liens 66-67 and 1)].

Therefore, it would have been obvious to one of ordinary skill in the art to combine Olarig (US 6,134,638) with Gustavson et al. (US 6,442,644) for the benefit of adjusting computer memory timing signals to obtain the invention as specified in claim 1.

27. As per **claim 2**, the combination of Gustavson and Olarig discloses "The system of claim 1" **[See rejection to claim 1 above]** "further comprising a process for measuring the distribution rate of the data strobe signal and the rate of a data bit arrival time across the memory component" **[Gustavson discloses this concept as "the controller monitors the specified DCLK for the transitions which accompany the responsive data burst to measure latency" (Column 40, lines 24-26)]**.

28. As per **claim 3**, the combination of Gustavson and Olarig discloses "The system of claim 2" **[See rejection to claim 2 above]** "further comprising a read data buffer operable for receiving the read data from the memory component and outputting the read data" **[Gustavson discloses this limitation as "data bus couples to a quartet of read latches, each 18 bits wide. These latches 540 are used for capturing read data output by gating unit 576" (Figure 5 and Column 45, lines 24-26). Gustavson further teaches this concept as "buffered modules permit deeper and/or wider memory configurations than the basic unbuffered configuration" (Column 40, lines 51-53) and explains that in a buffered mode, "a data-side"**

buffer is "interposed between data-sides of devices 340-350 and DataLink_B" (Column 41, lines 26-28). Olarig also discloses this limitation as "data read from the memory array to the system processor is preferably stored temporarily in one of the data buffers 0, 1 in queue read buffer. Data is placed in data buffers 0 and 1 by memory control 206 and read out by processor control 202" (Column 8, lines 50-54)].

29. As per **claim 4**, the combination of Gustavson and Olarig discloses "The system of claim 1," **[See rejection to claim 1 above]** "further comprising: a finite state machine (FSM) operable for determining the rank of at least one memory component from an address associated with the data to be read from the memory component;" **[Gustavson discloses this concept as "a command module can send information-seeking, query packets to individually-addressable memory units for discovering their internal organization and basic characteristics" (Column 7, lines 26-30) wherein "examples of such internal organization information includes number of memory banks, number of memory rows per bank, number of memory columns per row, number of bits or words per column and number of parallel data output lines. Examples of basic characteristics include minimum and maximum latency times for accessing a specific column of a not-yet-opened row in a not-yet-opened bank" (Column 7, lines 31-40) and explain0s that "a bank read operation generally requires the selecting or opening of a specific bank, in combination of selecting or opening a specific row" (Column 20, lines 43-45) as associating a bank of a memory component with an address of data to be read from a memory component. Gustavson further discloses "The specific command packet depicted in Table 2.0 is designed for individually addressing up to 256 IAMU's (individually-addressable, memory units) where each such IAMU can have as many as 8**

banks of DRAM storage, with each bank having as many as 1024 individually addressable rows of DRAM storage, and each row having as many as 128 individually addressable columns of DRAM storage" (Column 31, lines 19-26)].

30. As per **claim 5**, the combination of Gustavson and Olarig discloses "The system of claim 1," **[See rejection to claim 1 above]** "wherein the memory component is a dual data-rate (DDR) memory component" **[With respect to this limitation, Gustavson discloses SLDRAM memory system which takes the advantage of DDR as "command/address words (each 10-bits wide) are synchronized consecutively with the rising and falling edges of a command clock that is provided as a differential pair of signals, CCLK and CCLK# on two, single-end terminated transmission lines 15b" (Figure 1A and Column 8, lines 40-44)]**.

31. As per **claims 6**, the combination of Gustavson and Olarig disclose the "The system/memory cell of claims 1," **[See rejection to claim 1 above]** "wherein the first portion adjusts the data strobe by multiples of a clock pulse, and wherein the second portion adjusts the position of the data strobe signal by fractions of the clock pulse" **[With respect to this limitation, Olarig discloses that "a number of frequency multipliers 501, 502 multiply the system clock frequency by a factor of n and m, respectively, where n and m may be any integer or fractional number. Similarly, dividers 504 divide their input frequency by any integer or fractional number p" (Column 11, lines 51-55)]**.

32. As per **claim 7**, the combination of Gustavson and Olarig discloses "The system of claim 1," **[See rejection to claim 1 above]** "wherein the second timing adjustment signal is operable for adjusting the data strobe signal" **[Gustavson teaches this concept as "the programmably-**

defined delays allow the controller 150 to accurately strobe in read data using the received DCLK signal" (Column 30, lines 34-36)].

33. As per **claim 8**, the combination of Gustavson and Olarig discloses "The system of claim 1," **[See rejection to claim 1 above]** "wherein the memory cells comprise: an adjustable pipeline for receiving second portion of the first adjustment signal;" **[Gustavson discloses this concept as "In the actual device, the tunable delay is usually established by vernier shifting of phases of internal clocks that strobe respective latches of the data pipeline instead of using analog delay elements. However, any kind of delay technology may be used as appropriate" (Column 20, lines 50-56) and explains that "a memory device may be divided into separate bank groups, each servicing a different DataLink and concurrent operation may be obtained with pipelined commands" (Column 50, lines 20-23) wherein "the in-circuit memory controller" is allowed to make "command adjustments (e.g. individual phase changes) to the delay elements such as 112a, b" (Column 21, lines 26-27) wherein "SLDRAM module 120' has its own set of separately tunable delay/phase means and its own set of SLIO receivers (*Synchronous Link Input/Output*) (for data read) and (for command receive)" (Column 22, lines 27-30)]** "a pulse stretch circuit for generating a gating signal for the data strobe signal;" **[With respect to this limitation, Gustavson discloses that "During read synchronization, the input data clock 696 is supplied to delay chain 660. Setting circuits 682 and 683 are operated to adjust the phases of their respective outputs 692, 693 such that the produced clock signal 695 has respective rising and falling edges that align as close as possible with optimal-detection, sampling points of the predefined synchronization signals" (Column 48, lines 15-20) and explains that "the delay of tunable**

BkRd delay element 112b may be increased by the command module 150' to provide a longer delay as appropriate for scheduling bank-read bursts" (Column 20, lines 40-48). Olarig further discloses this limitation as "synchronism is preferably accomplished by stretching a signal so that it is asserted for additional clock pulses" and explains that "timing synchronizer" includes "timing logic and two flip flops" (Column 7, lines 31-34)] "a logical gate for combining the gating signal with the data strobe signal from the memory component to produce a gated data strobe signal; a delay clock circuit operable for: imparting a predefined time delay on the gated data strobe signal; and adjusting the timing of the data strobe to coincide with the data pulse;" **[Gustavson teaches this concept as "Buffer 619 couples the master clock 610 to a first input of a multi-tapped DLL (delay locked loop). An end-tap of DLL 620 is coupled to its feedback input. There is a voltage-controlled delay or a like variable delay means within DLL 620. (See for example DLL 620' of FIG. 6B) Internal controls within DLL 620 modulate the variable delay until successive rising edges at the feedback input are in phase with the rising edges of the master clock 610" (Figure 6 and Column 46, lines 17-25) wherein "a signal 622 which defines the locked delay amount of DLL 620 is coupled to a like-designed unit 640" (Column 46, lines 30-31). Gustavson also explains that "Initialization unit 641 couples to the plural taps of variable delay unit 640" and that "To make these phase adjustments, initialization unit 641 connects an initialization-selected first of the taps of unit 640 to output line 642 for defining the phase of rising edges supplied to clock input 646. Initialization unit 641 further connects an initialization-selected second of the taps of unit 640 to output line 643 for defining the phase of falling edges supplied to clock input 646" (Column 46, lines 38-57)]** "and a logic gate for

reading out the data" **["data bus couples to a quartet of read latches, each 18 bits wide. These latches 540 are used for capturing read data output by gating unit 576" (Figure 5 and Column 45, lines 24-26)]**.

34. As per **claim 9**, the combination of Gustavson and Olarig discloses "The system of claim 1," **[See rejection to claim 1 above]** "wherein the table is located in a memory controller hub (MCH)" **[With respect to this limitation, Gustavson discloses "The controller monitors the specified DCLK for the transitions which accompany the responsive data burst to measure latency. Once the minimum latencies have been measured for each SLDRAM module, an appropriate read latency value can be calculated and programmed into each device by writing to its Read Delay Registers" (Figure 6 and Column 40, lines 24-29) as having latency information within a memory controller]**.

35. As per **claim 10**, the combination of Gustavson and Olarig discloses "The system of claim 1," **[See rejection to claim 1 above]** "wherein the table is located within the memory component" **[With respect to this limitation, Gustavson discloses having a table to define time adjustments as "device-internal registers and other memory may be used for storing local ID codes, calibration values and other information" wherein device characteristics information comprises "number of banks" and "delay values" (Table 2.5 and Column 37, lines 55-63) and explains that "in response to command module 150' placing a code representing the current frequency of CCLK in the 'Frequency register' of a given SLDRAM module, the latter module will generally alter the characteristic information (e.g., min/max delay times) it provide on the read-only side of its LCM (*local configuration memory*)" (Column 38, lines 56-61)]**.

36. As per **claim 11**, Gustavson discloses "A method, comprising: calculating the rank of the DDR memory component from a command tenure;" **[Gustavson discloses this concept as "a command module can send information-seeking, query packets to individually-addressable memory units for discovering their internal organization and basic characteristics" (Column 7, lines 26-30) wherein "examples of such internal organization information includes number of memory banks, number of memory rows per bank, number of memory columns per row, number of bits or words per column and number of parallel data output lines. Examples of basic characteristics include minimum and maximum latency times for accessing a specific column of a not-yet-opened row in a not-yet-opened bank" (Column 7, lines 31-40)]** "and using the at least one timing adjustment signal to adjust a gating circuit for gating a data strobe signal to account for timing variations for reading data in a memory component" **[With respect to this limitation, Gustavson discloses "the use of a non-free running strobe (DCLK's) for capturing data or information in a memory system whereby the strobe has a preamble of edge transitions prior to the data is advantageous in that it allows the receiving device to lock onto the strobe frequency, and to compensate for internal delays of the latching signals in the receiving device, and/or to reduce intersymbol interference of strobe signal and thereby reduce timing uncertainty" (Column 52, lines 24-32). Gustavson also discloses a "fine-and-coarse tunable delay element of fig. 1b, namely 112b (BkRd) represents at least the latency delay of IAMU (*individually addressable memory unit*) 111 for a given bank read operation where the bank read operation generally requires the selecting or opening of a specific bank" wherein "the delay of tunable BkRd**

delay element 112b may be increased by the command module 150' to provide a longer delay as appropriate for scheduling bank-read bursts" (Column 20, lines 40-48)].

Gustavson does not disclose expressly "extracting at least one timing adjustment signal from a look-up table associated with the calculated rank."

Olarig discloses "extracting at least one timing adjustment signal from a look-up table associated with the calculated rank" as **["computer system 100 preferably allows communication with banks of SDRAM devices that require different clock frequencies, as well as other timing parameters. For memory PCI bridge controller to effectuate data writes to and reads from memory array, computer system must determine which types of SDRAM devices are present in the system memory. The memory type information to drive an appropriate clock signal frequency to each bank of SDRAM and to provide certain other timing parameters appropriate for each bank of memory chips" (Column 9, lines 39-50). Olarig also teaches that "memory clock generator includes BIOS data interpreter, bank speed control register, and memory timing control register" (Column 10, lines 38-40); having "BIOS data interpreter 510, which determines the appropriate memory clock frequency for the memory device and stores the clock frequency information in bank speed control register" (Column 10, lines 50-53 and Column 11, table II)]**.

Gustavson et al. (US 6,442,644) and Olarig (US 6,134,638) are analogous art because they are from the same field of endeavor of controlling timing signals used for computer memory access and control.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the computer memory system which applies timing adjustments to memory banks as

well as to components within each memory bank that calculates ranks of memory components as taught by Gustavson and further extract "at least one timing adjustment signal from a look-up table associated with the calculated rank" of a memory component as taught by Olarig.

The motivation for doing so would have been because Olarig teaches that applying timing adjustment signals for each memory rank and having a look-up table to store these timing adjustments **[provides the advantage of reducing computer system cost as consumers are able to "re-use" older "memory devices in new computer systems" when "upgrading to a new computer system" (Column 2, lines 39-42); providing a system that is "capable of implementing memory devices with different operating speed," therefore, optimizing the "performance of each memory device by performing transaction at the fastest possible speed with each memory circuit" (Column 2, lines 60-67) as "the memory clock signals may include different frequencies and thus allow different speed SDRAM's to be used in computer system" (Columns 4-5, liens 66-67 and 1)]**.

Therefore, it would have been obvious to one of ordinary skill in the art to combine Olarig (US 6,134,638) with Gustavson et al. (US 6,442,644) for the benefit of adjusting computer memory timing signals to obtain the invention as specified in claim 11.

37. As per **claim 12**, the combination of Gustavson and Olarig disclose "The method of claim 11," **[See rejection to claim 11 above]** "further comprising extracting a second timing adjustment signal from the look-up table associated with the calculated rank and memory component; and using the second timing adjustment signal to synchronize the gated data strobe signal with the data signal" **[With respect to this limitation, Olarig discloses "BIOS data interpreter 510, which determines the appropriate memory clock frequency for the**

memory device and stores the clock frequency information in bank speed control register" (Column 10, lines 50-53 and Column 11, table II) and explains that "if more than four memory clock frequencies are available in computer system 100, bank speed control register 520 can be expanded to include additional bits of speed control information. Table II defines the four possible clock frequencies for each bank of SDRAM devices given two bits of speed control definition in bank speed control register 520" (Column 10, lines 49-67)].

38. As per **claim 13**, the combination of Gustavson and Olarig discloses "The method of claim 11," **[See rejection to claim 11 above]** "wherein the command tenure comprises a read command and an address associated with the data" **[Gustavson discloses this limitation as "a bank read operation generally requires the selecting or opening of a specific bank, in combination of selecting or opening a specific row" (Column 20, lines 43-45) as associating a bank of a memory component with an address of data to be read from a memory component. Olarig also discloses this limitation as "it should be recognized that the speed at which the state machine 540 must match the speed of each SDRAM as each SDRAM is accessed for read or write cycles" (Column 12, lines 28-31)]**.

39. As per **claim 14**, the combination of Gustavson and Olarig discloses "The method of claim 11" **[See rejection to claim 11 above]** "wherein the at least one timing adjustment signal comprises a first portion and a second portion, wherein the first portion is used to grossly adjust the gating signal using integer multiples of a clock signal, and wherein the second portion is used to finely adjust the position of the gating signal using fractions of the clock signal" **[With respect to this limitation, Olarig discloses that "a number of frequency multipliers 501, 502**

multiply the system clock frequency by a factor of n and m, respectively, where n and m may be any integer or fractional number. Similarly, dividers 504 divide their input frequency by any integer or fractional number p" (Column 11, lines 51-55)].

40. As per **claim 15**, the combination of Gustavson and Olarig discloses "The method of claim 11," **[See rejection to claim 11 above]** "further comprising: shifting the gated data strobe signal by ¼ of a clock pulse" **[With respect to this limitation, Olarig discloses that "a number of frequency multipliers 501, 502 multiply the system clock frequency by a factor of n and m, respectively, where n and m may be any integer or fractional number (Column 11, lines 51-55). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to make "the predefined delay" as recited in claim 15 be specifically ¼ of a system clock pulse]**.

41. As per **claim 16**, the combination of Gustavson and Olarig discloses "The method of claim 15," **[See rejection to claim 15 above]** "further comprising: using the shifted data strobe signal to trigger a flip-flop for reading the data" **[With respect to this limitation, Olarig discloses that "data bus couples to a quartet of read latches, each 18 bits wide. These latches 540 are used for capturing read data output by gating unit 576" (Figure 5 and Column 45, lines 24-26)]**.

42. As per **claim 17**, Gustavson discloses "A memory cell; comprising: an adjustable pipeline operable for: of a first adjustment signal having a first value;" as **["a memory device may be divided into separate bank groups, each servicing a different DataLink and concurrent operation may be obtained with pipelined commands" (Column 50, lines 20-23) wherein "the in-circuit memory controller" is allowed to make "command adjustments**

(e.g. individual phase changes) to the delay elements such as 112a, b" (Column 21, lines 26-27) wherein "SLDRAM module 120' has its own set of separately tunable delay/phase means and its own set of SLIO receivers (*Synchronous Link Input/Output*) (for data read) and (for command receive)" (Column 22, lines 27-30). Note that delay elements 112b represent tunable delay elements associate with memory banks and delay elements 112a represent tunable delay elements associated with pages within each memory bank] "a pulse stretch circuit for stretching the gating signal in time;" **[With respect to this limitation, Gustavson discloses that "During read synchronization, the input data clock 696 is supplied to delay chain 660. Setting circuits 682 and 683 are operated to adjust the phases of their respective outputs 692, 693 such that the produced clock signal 695 has respective rising and falling edges that align as close as possible with optimal-detection, sampling points of the predefined synchronization signals" (Column 48, lines 15-20) and explains that "the delay of tunable BkRd delay element 112b may be increased by the command module 150' to provide a longer delay as appropriate for scheduling bank-read bursts" (Column 20, lines 40-48)]**"a logical gate for combining the stretched gating signal with a data strobe signal from a targeted memory component to produce a gated data strobe signal; a delay clock circuit operable for: imparting a predefined time delay on the gated strobe signal; and adjusting the timing of the delayed data strobe signal to coincide with the read data pulse;" **[Gustavson teaches this concept as "Buffer 619 couples the master clock 610 to a first input of a multi-tapped DLL (delay locked loop). An end-tap of DLL 620 is coupled to its feedback input. There is a voltage-controlled delay or a like variable delay means within DLL 620. (See for example DLL 620' of FIG. 6B.) Internal controls within DLL 620 modulate the variable**

delay until successive rising edges at the feedback input are in phase with the rising edges of the master clock 610" (Figure 6 and Column 46, lines 17-25) wherein "a signal 622 which defines the locked delay amount of DLL 620 is coupled to a like-designed unit 640" (Column 46, lines 30-31). Gustavson also explains that "Initialization unit 641 couples to the plural taps of variable delay unit 640" and that "To make these phase adjustments, initialization unit 641 connects an initialization-selected first of the taps of unit 640 to output line 642 for defining the phase of rising edges supplied to clock input 646. Initialization unit 641 further connects an initialization-selected second of the taps of unit 640 to output line 643 for defining the phase of falling edges supplied to clock input 646" (Column 46, lines 38-57)] "and a circuit for reading out the data" **[With respect to this limitation, Gustavson discloses "data bus couples to a quartet of read latches, each 18 bits wide. These latches 540 are used for capturing read data output by gating unit 576" (Figure 5 and Column 45, lines 24-26)]**.

Gustavson does not disclose expressly adjusting a timing signal by a fractional portion, nor "adjusting timing of a gating signal by a length of time equal to the value of the fractional portion of the first adjustment signal."

Olarig discloses adjusting timing signals by a fractional portion and "adjusting timing of a gating signal by a length of time equal to the value of the fractional portion of the first adjustment signal" as **[a system in which "the memory clock signals may include different frequencies and thus allow different speed SDRAM's to be used" having "memory clock generator" programmed "to provide an appropriate clock frequency based on" data that "identifies the type of SDRAM included in each bank" (Columns 4-5, lines 66-67 and 1-5).**

Olarig also teaches that "clock generator 500 preferably is provided with the system clock from which the clock generator derives SDRAM clock frequencies. A number of frequency multipliers and frequency dividers are used in conjunction with multiplexers 506, 530 for selecting an appropriate clock frequency" (Figure 6 and Column 11, lines 43-46) as being able to adjust timing signals by different amounts; for example, being able to produce a amount delay when multiplying or smaller amount when dividing by any integer].

Gustavson et al. (US 6,442,644) and Olarig (US 6,134,638) are analogous art because they are from the same field of endeavor of controlling timing signals used for computer memory access and control.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the computer memory system which applies timing adjustments to memory banks as well as to components within each memory bank as taught by Gustavson and further adjust timing signals by different amounts, including fractional amounts, as taught by Olarig.

The motivation for doing so would have been because Olarig teaches that adjusting memory control timing signals by different amounts, including fractional amounts **[provides the advantage of reducing computer system cost as consumers are able to "re-use" older "memory devices in new computer systems" when "upgrading to a new computer system" (Column 2, lines 39-42); providing a system that is "capable of implementing memory devices with different operating speed," therefore, optimizing the "performance of each memory device by performing transaction at the fastest possible speed with each memory circuit" (Column 2, lines 60-67) as "the memory clock signals may include different**

frequencies and thus allow different speed SDRAM's to be used in computer system" (Columns 4-5, liens 66-67 and 1)].

Therefore, it would have been obvious to one of ordinary skill in the art to combine Olarig (US 6,134,638) with Gustavson et al. (US 6,442,644) for the benefit of adjusting computer memory timing signals to obtain the invention as specified in claim 17.

43. As per **claim 18**, the combination of Gustavson and Olarig discloses "The memory cell of claim 17," **[See rejection to claim 17 above]** "wherein the delay clock circuit is further operable for receiving a second adjustment signal having a predefined value; and using the predefined value of the second adjustment signal to adjust the time of the delayed data strobe signal" **[Gustavson discloses this concept as "a signal 622 which defines the locked delay amount of DLL 620 is coupled to a like-designed unit 640" (Column 46, lines 30-31). Gustavson also explains that "Initialization unit 641 couples to the plural taps of variable delay unit 640" and that "To make these phase adjustments, initialization unit 641 connects an initialization-selected first of the taps of unit 640 to output line 642 for defining the phase of rising edges supplied to clock input 646. Initialization unit 641 further connects an initialization-selected second of the taps of unit 640 to output line 643 for defining the phase of falling edges supplied to clock input 646" (Column 46, lines 38-57)]** "and a logic gate for reading out the data" **["data bus couples to a quartet of read latches, each 18 bits wide. These latches 540 are used for capturing read data output by gating unit 576" (Figure 5 and Column 45, lines 24-26)]**.

44. As per **claims 19**, the combination of Gustavson and Olarig discloses "The memory cell of claim 17," **[See rejection to claim 17 above]** "wherein the predefined delay is equal to ¼ of a

system clock pulse" **[With respect to this limitation, Olarig discloses that "a number of frequency multipliers 501, 502 multiply the system clock frequency by a factor of n and m, respectively, where n and m may be any integer or fractional number (Column 11, lines 51-55). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to make "the predefined delay" as recited in claim 19 be specifically ¼ of a system clock pulse]**.

45. As per **claim 20**, the combination of Gustavson and Olarig discloses "The memory cell of claim 19," **[See rejection to claim 19 above]** "wherein the value of the fraction portion of the first adjustment signal comprises a fraction portion of the system clock pulse" **[With respect to this limitation, Olarig discloses that "a number of frequency multipliers 501, 502 multiply the system clock frequency by a factor of n and m, respectively, where n and m may be any integer or fractional number. Similarly, dividers 504 divide their input frequency by any integer or fractional number p" (Column 11, lines 51-55)]**.

VI. RELEVANT ART CITED BY THE EXAMINER

46. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

47. The following references teach applying timing adjustments to memory components.

U.S. PATENT NUMBER

US 6,208,563

US 6,715,096

US 5,577,236

US 5,623,638

US 2003/0145162

US 6,496,906

VII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

48. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

49. Per the instant office action, claims 1-20 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

50. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

51. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 3, 2006

Yaima Campos
Examiner
Art Unit 2185

DONALD SPARKS
SUPERVISORY PATENT EXAMINER